

The Road Ahead

Roads not taken

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■ **IN ITS FOCUS** on embedded memories, the *Design & Test* January/February 2011 issue also included several articles on the prospects for resistive RAM (RRAM), spin-transfer torque magnetoresistive RAM (STT-MRAM), and phase-change RAM (PCRAM). Against that backdrop, it is interesting to consider recent conclusions of the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) technology working groups within the *International Technology Roadmap for Semiconductors*. (I thank my ITRS colleagues Jim Hutchby and Mike Garner, who chair the ERD and ERM working groups, for providing an advance copy of their *Future Fab* article, http://www.future-fab.com/content/PDF/FF36_Jan_11.pdf, from which I liberally quote in this column.)

In a July 2010 workshop report (http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/ERD_ERM_2010FINALReportMemoryAssessment_ITRS.pdf), Hutchby and Garner describe a multiyear “assessment of eight memory technologies to determine whether one or more should receive increased focus to accelerate technology development toward commercialization.” The report states: “To be considered for increased focus, the memory technology needs to have demonstrated good performance with an understood storage mechanism and be scalable multiple generations beyond the 16 nm technology generation. Further, it should be ready for manufacturing within the next 5 to 10 years.

“After reviewing white papers on each memory technology, the cases for each technology were presented by advocates and challenged by ‘friendly critics’. Following review and discussion, the ERD and ERM Work Groups recommended to the IRC [International Roadmap Committee] that STT-MRAM and Redox [reduction/oxidation] RAM receive additional focus in research and development to accelerate

progress toward commercialization of one or both of these technologies.” The workshop report and the *Future Fab* article by Hutchby and Garner together document a significant recent example of industry-wide processes that lead to “roads not taken.”

Obtaining industry consensus on what *not* to do—what road not to take—is a critical aspect of achieving consensus and focus on what *to* do. Over the past decade, I have worked with a US-based consortium on several studies that have sought to quantify “research funding gaps” worldwide. Such studies, even when simplistic, can be eye-opening. Suppose, for instance, that the semiconductor industry must fulfill a specific technology requirement—for example, “discover a Flash memory replacement for sub-16-nm technologies.” For any given technology requirement, there may be five potential solutions. There may be three major world regions (North America, Asia, Europe) pursuing each potential solution at any given moment. To make progress on a potential solution requires a critical mass of research effort from at least three professors and a dozen PhD students. Each researcher requires, say, \$200,000/year in support for salary and equipment.

It’s soon obvious that tens of millions of dollars of research funding per year are required to address *each* technology requirement. (Two exercises for the reader come to mind at this point. First, at its peak, how many dollars per year did the US National Science Foundation spend on VLSI design and test research? Second, what is the average amount of research funding available from consortia such as MARCO or SRC for each “red brick” [i.e., technology requirement with no known solutions] in the ITRS?) In this light, it is highly significant that two out of the eight potential next-generation memory technology

solutions identified in the 2009 ITRS have now been recommended to receive increased R&D focus.

Returning to those candidate memory technologies: Just what did the ITRS ERD and ERM working groups—many hundreds of R&D experts worldwide—consider in their years of workshops and evaluations? Above all, *they applied a manufacturer's perspective*. Some of the groups' evaluation criteria, which I excerpt here from the Hutchby and Garner *Future Fab* article, follow:

- Physics of operation addressing factors determining the operating voltage; ultimate time constant for changing the state; ultimate time to read the state; retention time of the state; amount of energy to change the state; and number of memory cycles (endurance).
- The potential for scaling the technology for multiple generations beyond the 16-nm generation. Questions to be answered: What are the limits of scaling? Are there intrinsic statistical fluctuations that could limit scaling?
- CMOS compatibility for stand-alone and embedded applications.
- Minimum number of mask layers or photolithographic steps to fabricate the device.
- A plausible means of fabricating a crossbar array and related circuits, including potential for multiple bits per memory layer and the potential for 3D integration of multiple memory layers.
- Key scientific and technological issues that must be addressed to realize the technology's full potential, including intrinsic material defects that could affect operation and reliability; extrinsic defects generated in operation that could affect operation and reliability; environmental interactions that could affect operation; material interfaces that must be controlled; parasitic properties that may limit the technology (leakage current, capacitance, etc.); factors that could limit density or future scalability; and factors that impact embedding the technology on a CMOS chip.
- A draft technology roadmap for the technology suggesting a 10-year development path for the specific device technology proposed, with its initially becoming manufacturable within the next 5 to 10 years (the 2016–2021 time frame).

The attractions of STT-MRAM cited by Hutchby and Garner are as follows: “1) a simple integration

scheme with the backend CMOS process; 2) by adding only three to four additional masks, the process requires no front-end device integration that interferes with the CMOS devices and no high-voltage devices; and 3) the STT-MRAM cell may be integrable with a vertical MOSFET select transistor, thereby reducing the footprint of the memory cell from $21F^2$ (current value) to $4F^2$.”

On the other hand, there were also challenges cited for STT-MRAM: “First and foremost is the ability to scale STT-MRAM to obtain a competitive cost/bit together with adequate performance parameters. The footprint or cell size of the STT-MRAM is determined by the layout of the select transistor, which, in turn, must be wide enough to provide the required program current. Consequently, the program current, which drives the power dissipation and the dimensional scaling of the STT-MRAM cell, must be reduced to $< 50 \mu\text{A}$ (ideally $\sim 10 \mu\text{A}$) to be competitive as a cost/bit technology. Furthermore, its switching speed is rather slow, and its meaningful application to logic that is highly scalable beyond CMOS is seen as very difficult. Another challenge is that the STT-MRAM cell structure requires 10-12 different layers, deposited by physical vapor deposition processes for a thickness of $\sim 0.8\text{--}2.0 \text{ nm}$.” (For details of the attractions and challenges of Redox RRAM, please see the *Future Fab* article at the aforementioned link.)

WHETHER FOR DEVICE architectures or next-generation lithography, back-end-of-line dielectric materials or test equipment standards, the story of semiconductor technology is just as much a story of roads not taken as it is one of roads taken. The story of how a community—representing a manufacturing and process, more than a design and test, perspective—of hundreds of R&D experts worldwide decided to recommend two roads in particular is a fascinating complement to the outlooks presented in *Design & Test's* January/February issue. ■

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