

DFM Challenges and Practical Solutions in 65nm and 45nm

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INTRODUCTION

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Agenda

- 0930-1000 Introduction (Kahng)
- 1000-1100 Test Structures, Test Chips, Design Style for 65nm, 45nm (Smayling)
- 1100-1130 Break
- 1130-1300 Interconnect Process Variations and RC Extraction (Nagaraj)
- 1300-1430 Lunch
- 1430-1600 Challenges and Opportunities for Design in Nano-CMOS Technologies (Wong)
- 1600-1630 Break
- 1630-1745 Manufacturing-Aware, Model-Driven Design Optimizations at 65nm and 45nm (Kahng)
- 1745-1800 Final Q&A

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Note: Updated slides at <http://vlsicad.ucsd.edu/>

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What's New in EDA tools for DFM (Schoellkopf, STMicroelectronics, DAC-06)

- **Big Foundry gives access to its “fab data” through encrypted standard format. Any CAD tool can now read those previously “secret” data to implement:**
 - Critical Area Analysis (and corrections)
 - Lithography Compliant Checks (and corrections)
 - CMP Checks (for parasitic extraction and dummy fill)
- **EDA and Foundries+IDMs collaborate for win-win situation: help the designer to get better chips (better yield, less power, more accurate timing) from manufacturing.**
- **More and more tools are DFM-aware:**
 - Litho-aware routers
 - Litho-aware and CMP-aware RC extractors
 - Variability handled by Statistical approach (Timing Analysis)

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What's New in EDA tools for DFM (Schoellkopf, STMicroelectronics, DAC-06)

- **Lithography Simulators, like DRC tools, are now ready for new computer architectures (multi-thread, multi-core, multi-processor)**
 - Can handle bigger designs in shorter times
 - Can do incremental modifications
 - Can do more verifications
- **At 90nm, Timing Closure was (is) the challenge**
- **At 65nm, DFM Closure is (already) the challenge**

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DFM Activity In Academia

■ Moving from the mechanics of SSTA to the question of how to feed statistical design tools

- This is a very tough issue
- More work on test structure design, and how to extract useful variational or process models from measured data
- Some “open model” kinds of initiatives

■ Rediscovering the issue of “closing the loop” between lithography simulation and electrical performance

- Goal = “shape-to-electrical” transform that builds on existing LPC (litho process check), hotspot finding, etc. litho-sim capability
- Again, this is a very tough issue → **e.g., What happens to SPICE corners !?!**

■ “Grand unification” of DFM/DFY with test getting traction

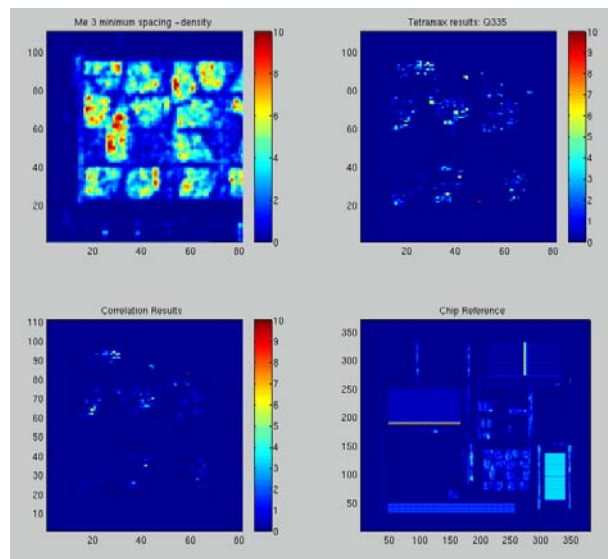
- Lots of data in the fab's YMS (yield management system) that remains unconnected to design issues such as constraints and signoff.
- Mismatches between silicon and models / signoff analyses are very costly
- **Eventually, need to be able to modulate the process to fit the design sweet spot (rather than only the other way around)**

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Example: Hot Spots versus Volume Diagnosis



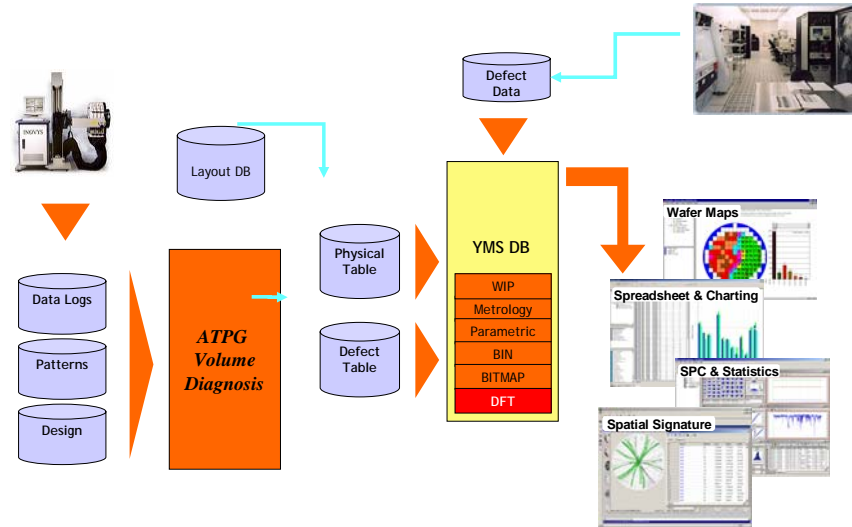
Courtesy of Davide Appello, ST (DFM&Y 2006)

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Picture of Test-DFM Closure



Courtesy of Davide Appello, ST (DFM&Y 2006)

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DFM Activity In Academia

■ Many new concerns and distractions

- Reliability (TDDDB, NBTI, SEU, ...) = concern
- Stress = concern
- Beyond-CMOS = distraction
 - CNTs
 - Bio-chips
 - QCAs
- "More Than Moore" = critical, but not so much in scope of DFM
 - Stacking/3D/SIP integration
 - Microarchitecture (multi-core, networks on chip)
 - Memory hierarchy
 - Design productivity (convergence, QOR, ...)

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DFM Activity In Industry

■ Foundries are thinking about opening up ... slightly

- TSMC DDK (DFM Design Kit), Open Model Initiative, ...
- Goal: allow fabless customers to access data in encrypted / arm's-length ways
- **Issue:** Metrics, competition/IP, business contract w/fabless
- **Issue:** SPICE model and RCX model guardbanding

■ First wave of DFM “golden validations” has arrived

- CMP simulation, litho simulation, critical area analysis, etc.
- In theory, lays groundwork for new optimizations that don't necessarily need expensive silicon experiments to be seen as having value.
- Integrated simulators (litho, CMP) will be provided/supported by foundries to enable accurate prediction of performance
 - “Process-Aware Timing” flows, etc. → **but these are currently broken !!!**
- **Issue:** what is the ROI from using such tools?
- **Issue:** SPICE, RCX guardband for signoff !!!
 - “Process-Aware Timing”: foundry must sign up to variant BC, WC corners!
 - With new “golden validations”: greater manufacturing-friendliness (RDR, CMP) gets rewarded by the fab? (tighter timing, power corners in signoff?)

DFM Activity In Industry

■ Some silicon successes for DFM

- Still mostly in IDMs
- Specialized products (high-volume custom): memory, FPGA, etc.

■ Understanding that analysis or simulation alone is not showing enough value

- → DFM companies moving towards optimization
- Electrical and performance issues at the forefront
- Highest value comes from combining electrical + optimization
- Leakage still a dominant concern

■ RDRs (radically restricted design rules) cause unnecessary discussion of value proposition of DFM

- With RDRs, will variation decrease so that DFM will not be needed?
- No solid method of measuring cost vs. benefit from RDRs
- Still see resistance to RDRs in 45nm consumer (LP) processes
 - Density and cost are still drivers
- 32nm almost certainly requires RDRs (even with many costly tricks)

The Way Things Were

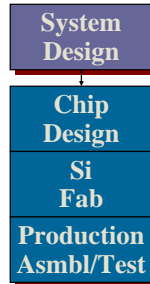
■ Trend for de-verticalization of the Industry

- Business Trade Offs : economy of scale vs. control
- Technical Trade Offs : core competence vs. integration

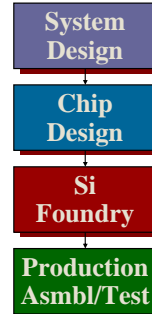
Vertical Entity



IDM



Fabless/Foundry



■ Foundry-Fabless Model Enabled by Commoditization

- e.g. General purpose process technology to service many product lines
- e.g. Standard (practical) handoffs between process and design

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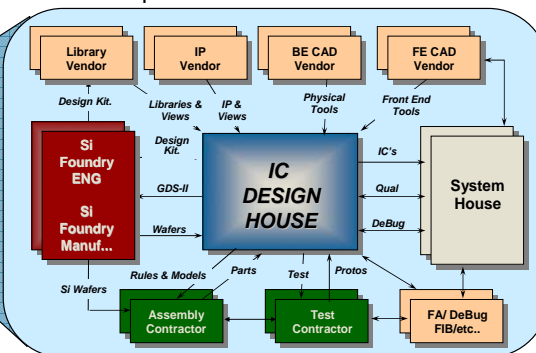
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Fabless Model is a Bit More Complicated

■ Extensive Interface Management Challenges

- Managing a diversity of business models in a supply chain
- Managing a diversity of technical specialties

Fabless/Foundry



■ The Real Challenge is When Things do not Work

- Ultimately the Chip House "holds the bag"
- Not a show stopper in established technologies and design flows because things mostly work

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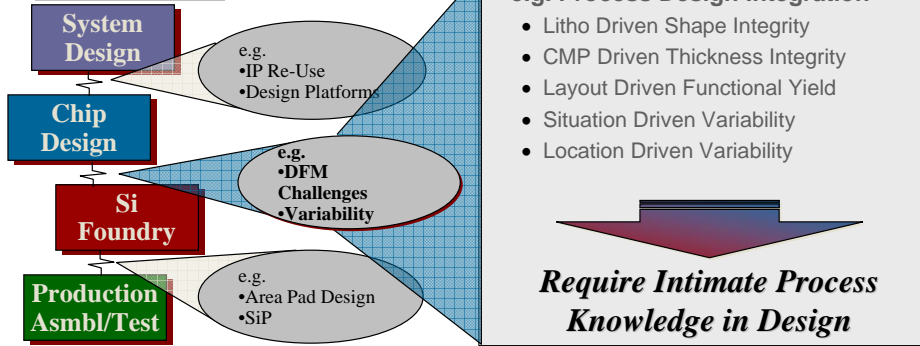
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Challenges at the Leading Edge

■ Growing Integration Challenges with Traditional Fabless Model

- Technical Challenges : Process-Design Integration at ~65 and below
- Business Challenges : cost of design on (b)leading edge

Fabless/Foundry



■ e.g. Process Design Integration

- Litho Driven Shape Integrity
- CMP Driven Thickness Integrity
- Layout Driven Functional Yield
- Situation Driven Variability
- Location Driven Variability

Require Intimate Process Knowledge in Design

■ At Advanced Nodes it is Increasingly Hard to Make Things Work

- And the business pressures do not make trade offs any easier
- It would seem that IDM model has an intrinsic technical advantage

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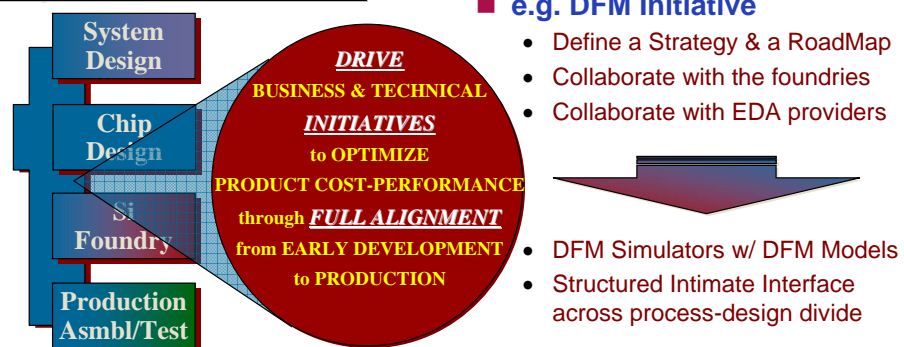
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Integrated Fabless Manufacturer

■ Integrating and Aligning the Supply Chain

- Technical Challenges : coordinated development to optimize a product
- Business Challenges : supporting a collaborative effort

Integrated Fabless Manufacturer



■ e.g. DFM Initiative

- Define a Strategy & a RoadMap
- Collaborate with the foundries
- Collaborate with EDA providers
- DFM Simulators w/ DFM Models
- Structured Intimate Interface across process-design divide

■ Aligned Technology Chain : through collaboration NOT ownership

- Best of Both Worlds : Business advantages and flexibility of the fabless world with technical alignment and integration of the IDM world

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The Way Things Are

■ Bifurcation of the Traditional Fabless Model : IFM

- Required for leadership on the leading edge
- Best of Both Worlds

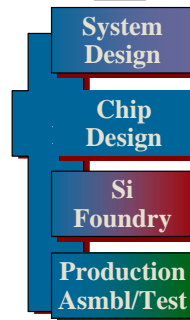
Vertical Entity



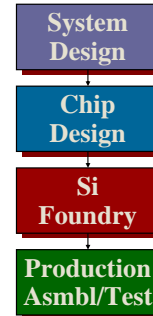
IDM



IFM



Fabless/Foundry



■ Integrated Fabless Manufacturer

- An approach for leadership in the fabless sector
- Good for Qualcomm, good for the industry

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DFM Survival Principles

■ Don't assume what doesn't exist

- "detailed process information", "statistics" to feed statistical tools, ...

■ Manufacturing process is not stable

- Try to use trends rather than numbers

■ Preserve the flow!

- Design teams already spent \$MM to make production flows
- Generalization: Don't mess with anything that's golden

■ Don't make improvements that aren't significant enough to be measured

- Full silicon A-B experiment costs ~\$2M
- Simulation is never sufficient proof

■ Separation of concerns is a good thing

- Don't assume "new silicon IC designer" (= deep + broad)
- → Abstract interfaces (rather than "break down barriers")

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DFM Reality Checks

- Communication of variation will be simpler and later than anticipated
- Designers and foundry also solve the problem!
 - Regular layout practices (e.g., on device layers)
 - Fab continuously reduces variation – ECMP, RDR, ...
- Size of opportunities is misunderstood
 - How much variation is systematic intra-/inter-die?
 - How different is the statistical optimization result from the deterministic optimization result?
- Difficult modeling / infrastructure challenges
 - E.g., correlation model that says 1 buffer = 2 inverters?
 - ‘Deconvolution’ problems (RCX/CMP, LPC/LPE, ...)

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Key Issues to Track Going Into 45nm and Beyond

- **Business**
 - Value proposition / ROI for adoption of DFM by design teams
 - Consensus on models, DFM-score, etc. standards
 - Correctly working and usable flows (integrated platforms)
 - Migration path to those flows
- **Technology**
 - Parametric yield optimization becomes a reality
 - DFM/DFY connections to YMS, DFT (e.g., silicon-signoff correlation)
 - Stress modeling and exploitation
 - DFM for the interconnect stack (BEOL)
 - Much more DFM in floorplan, physical synthesis, P&R (+ analysis support)
 - Support for restricted layout
 - Guardband reduction
 - Improved routers
 - 32nm support: Layout decomposition or grating-based layout
 - Lots of “connecting the dots” (CMP, litho, CAA, device performance, device reliability, ...)

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What Else?

- What are the key trends and questions in YOUR view?
- Moving DFM up in the design chain – e.g., to functional level (before physical level)
- DFM at fault analysis stage – how to correct current design?

■ _____

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